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Design of Multi Bit Flip Flop in FIR Application Using Clustering Algorithm

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***Abstract*- In Integrated Circuit industry power has become a major contribution. The main attribute is the clock power in circuits of VLSI. In today's VLSI design scenario, power utilization by clocking takes up a vital role especially in design that uses deeply scaled CMOS technology. Proficient power utilization tends to be an important constraint in modern IC design. The underneath idea of multi bit flip flop is to reduce the inverter number by sharing among flip flop. Indulging multi bit flip flop in synchronous design is becoming a considerable method for reducing clock power. The single bit flip flop cells uses a mutual number of inverter that possess high driving capability to drive over clock signal. Grouping of such cells to form multi bi flip flop can spare drive strength, dynamic power and area of common inverter where there is no compromise among the necessary constraint among area and power. In this paper, a Hausdorff clustering algorithm is utilized to obtain nearest clustering for merging flip flops. The multi bit technique is introduced in FIR circuit to lessen power as well as area. This satisfies with the above given constraints. According to the experimental results, our algorithm significantly reduces clock power by 25.8% and it is found that total gate count is reduced from 186 to 128. The delay is curtailed upto 1.19 ns which increases the speed.**

Keywords- Clock Power, Cluster, Delay, Manhattan Distance, Merging, Multi Bit Flip Flop

I. INTRODUCTION

As power consumption is the key factor, where the compromise of it cannot be done. This has been an important facet that regards with performance constraint. Due to high switching activity 20-45 % of chip power is consumed by flip flop themselves [1].

$$P_{clk} = C_{clk}V^{2}_{dd}f_{clk} \quad (1)$$

Where P_{clk} is clock power, f_{clk} is the clock frequency, V_{dd} is the supply voltage and C_{clk} is the switching capacitance including gate capacitance of flip flops. Clock distribution and generation circuitry is acclaimed to consume upto 40% and 36% of the total power budget of current high performance and reduce battery life [2]. Clock network has been given in terms of its timing performance [3] and of its power impact [4]. In reducing power consumption of SOC, clock network plays dominant role as it accounts for upto 50% [5] of dynamic power in some real circuits. Many kinds of power reduction techniques have been proposed. Clock power minimization on buffer sizing for skew constraints[6].In the placement stage power of clock network has been minimized [7], [8] by considering the location of registers. Registers are grouped into clusters. To reduce wirelength registers are placed very closer in a cluster. Many low power design techniques have been introduced [9] to optimize power consumption such as clock gating [10], [11]. Power aware placement flow [12] generates register banks based on predetermined heuristic criteria after initial placement and eliminates generated register banks to satisfy timing and routability constraints during incremental placement optimization. For more accurate timing/delay budgets, to optimize a design with multi bit flip flops at post placement stage.

The previous works [13] for post placement optimization with multi bit flip flops. Based on different design objectives alienated three phase approach to obtain power saving. To minimize number of clock sinks and net switching power is proposed. Total wire length is reduced and net switching power is minimized [14] during MBFF placement by clique based approach. To utilize multi bit flip flop for clock power under consideration of timing and forbidden region constraints [15] greedy based merging approach is used. It shows MBFF in a cell library are neighboring in the bit number. Under the constraints of placement density and timing slack [16] progressive window based approach to merge 1-bit flip flop into multi bit flip flop.

This paper is organized as follows. Section I dealt about the concepts of using merging flip flop. Section II explains the working of multi bit flip flop. Section III describes about the design flow of the proposed method. Section IV gives simulation results in FIR application using hausdorff algorithm. Section V describes the performance analysis. Conclusion of the work is explained in section VI.

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II. MULTI BIT FLIP FLOP

The logic diagram of a single bit flip flop consist of one master latch, one slave latch and one clock driver as illustrated in Figure2. In four bit flip flop one common clock driver is shared for both master and slave latch. Six inverters in a 4 one-bit flip flop can be eradicated in a 4- bit flip flop. As a result, two 1-bit flip flop will consume more power than one 2-bit. And also 4-bit flip flop occupies a smaller amount of area than four 1-bit flip flops. As technology advances to nano and micro, even a minimum size inverter [17] can drive more number of latches.

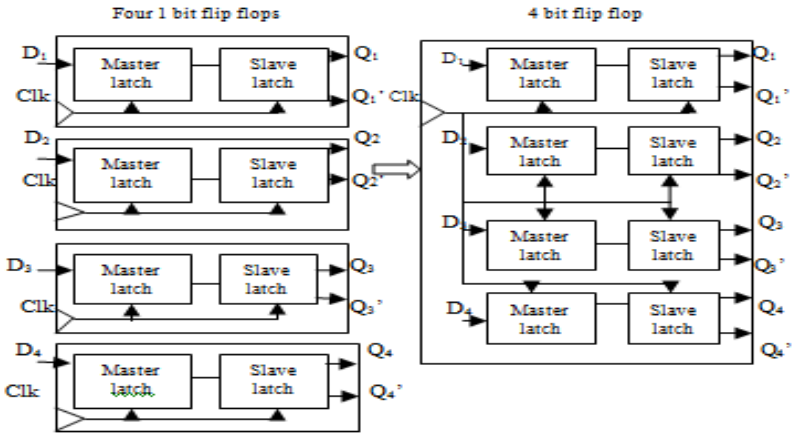


Figure 1. Merging 4 1-bit flip flop into 4 bit flip flop

III. PROPOSED SYSTEM

The projected style flow is roughly categorised into 5 stages as shown in Figure 3. Within the starting, we tend to construct D flip flops that every flip flop will handle single bit data. the gap of every flip flop is calculated by manhattan distance. Manhattan distance computes every flip flop distance. Distance values found by manhattan function. From the distance values, Clustering will be formed using hausdorff algorithm. Then combination table is designed. From the data together table merging is done.

A. Initialize D latch

A master slave D-FF of each handles single bit data input. A master–slave D flip-flop is created by connecting two gated D latches in series, and inverting the enable input to one of them. This flip-flops gets single bit as input and generate output as Q and Q`. At a time any one of D flip-flop was activated according to clock pulse generation. These flip flops have single input and separate clock signal generator for each.

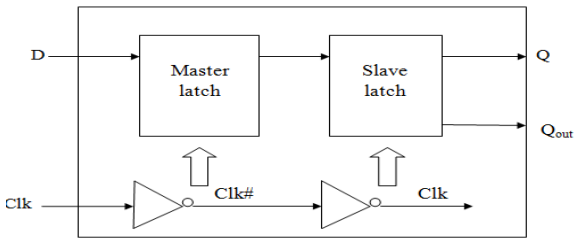


Figure 2. Single bit flip flop

B. Calculate Distance

We find the distance between the neighboring flip flops which gets the distance between each flip flops. This distance calculation was done by Manhattan distance function. Manhattan distance function computes the distance that would be traveled to get from one data point to the other if a grid-like path is followed. The formula for this distance between a point **F** = (**F**1, **F**2, etc.) and a point **G** = (**G**1, **G**2, etc.)

$$d = \sum_{i=0} n \left| F_i - G_i \right| \quad (2)$$

Where n is the number of variables, and **F**i and **G**i are the values of the ith variable, at points **F** and **G** respectively.

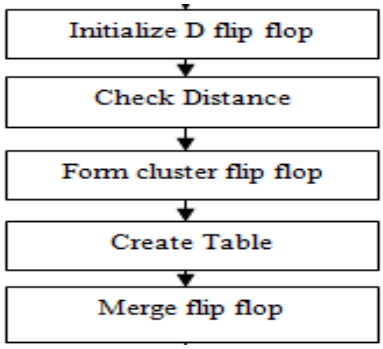


Figure 3. Proposed System

C. *Form Cluster*

After finding the distance between the flip flops we form flip flops in clusters according to the distance information. This clustering represents what are the flip flops can be made to merge and form as a multi bit flip flops. This clustering was found by Hausdorff Clustering algorithm to form clustered flip flop.

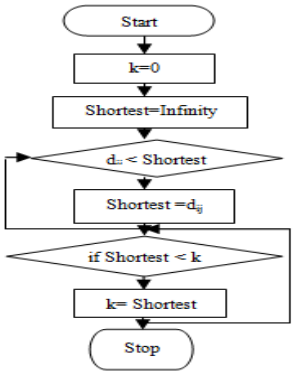


Figure 4. Flowchart of hausdorff algorithm

Fig. 4 gives the flowchart of clustering algorithm. Initially k is zero. Shortest is taken as infinity. The first distance value is taken and it is checked for the shortest, whether the distance value is less than shortest. If it is true, distance value is assigned to shortest, otherwise there is no change in the shortest. The next condition, if shortest is greater than k, then k tends to be the shortest. The loop will execute for all the distance values. Fig. 5 demonstrates insight block view.

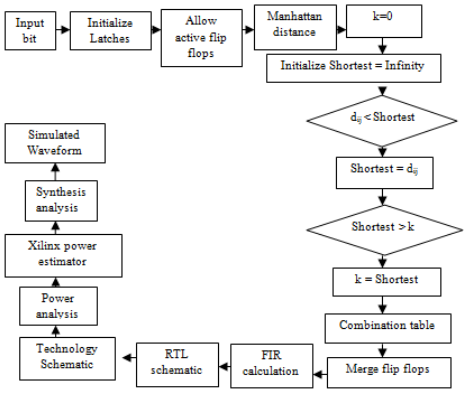


Figure 5. Insight block

D. *Comination Table*

After cluster formation, combination table is created which contains the cluster information of each flip flop. From this, decision was taken to merge flip flops. Then from this information, we can merge flip flops.

E. *Merge Flip Flops*

Merging flip flops means giving same clock pulse to several flip flops within the same cluster, thus reducing area and power consumption. The wirelength is greatly reduced.

IV. Simulation Results And Discussion

This section describes simulation result. The experiment is carried out using Xilinx ISE Design Suite 14.2 keeping Spartan 3E-XE3S500 as the target device . The performance analysis is given in table I. Usually the FIR circuit results an overhead in power but by using the proposed method it is found that 19.8% of total power is reduced, it is also found that the total gate count is reduced from 176 to 132 compared to the design without using merging concept. The speed of algorithm is increased with the delay reduction of 1.9 ns. The simulated waveform is shown in Figure7.

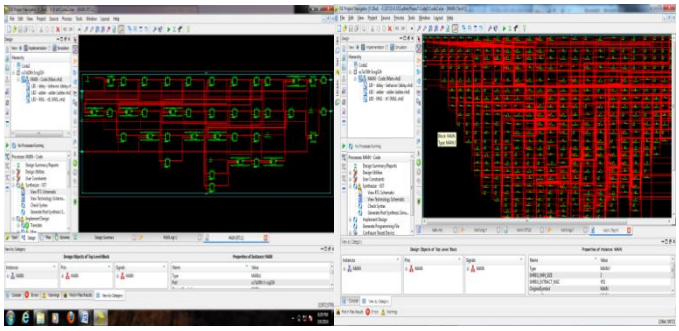


Figure 6. (a) RTL schematic (b) Technology Schematic

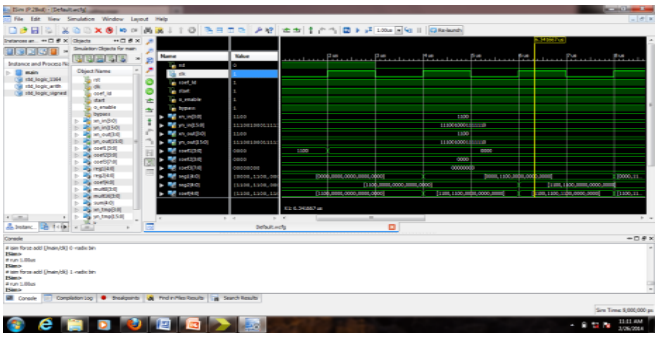


Figure 7. Simulated Waveform

In Fig. 6, RTL and technology schematic for FIR circuit is shown. Power consumption of FIR circuit after using clustering algorithm and merging concept is shown in Figure 7.

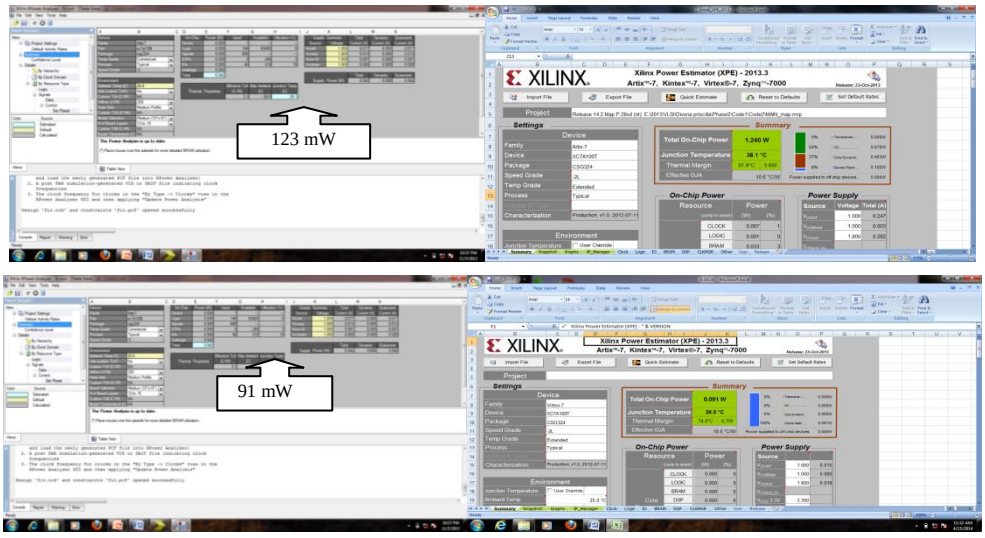


Figure 8. Power consumption (a) before and (b) after merging

Delay is analysed in Figure 8 and thus speed is calculated with inverse of delay. It is found that speed is increased with the delay reduction.

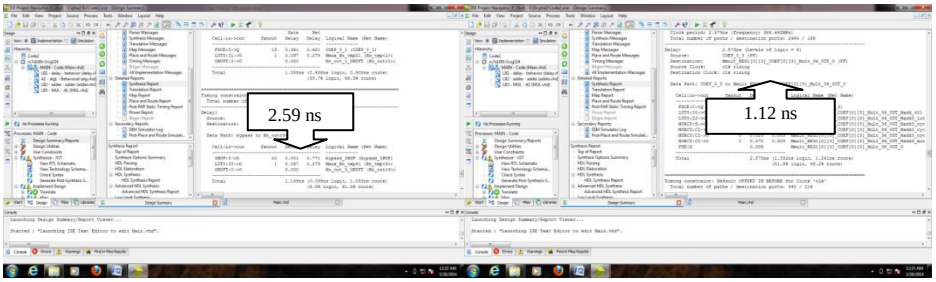


Figure 9. Delay value (a) before and (b) after merging

The area reduction is considered with the number of flip flops in the FIR circuit is given in Figure 9.

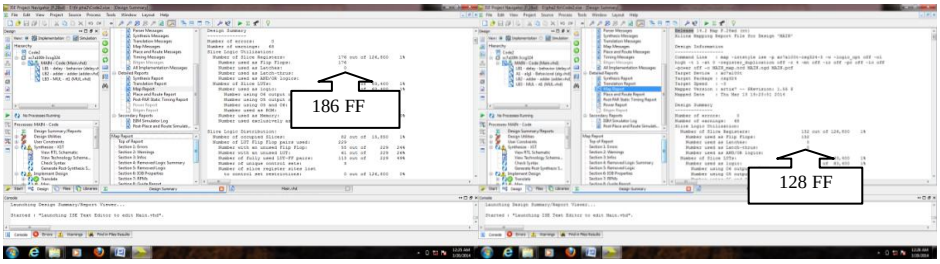


Figure 10. Area usage (a) before and (b) after merging

Peak memory usage is given in Figure 10 with the reduction from 391 MB to 389 MB. Figure 11 shows the graphical representation of performance analysis.

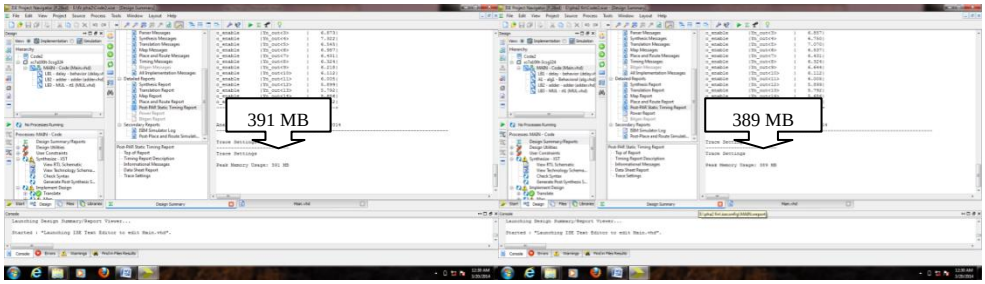


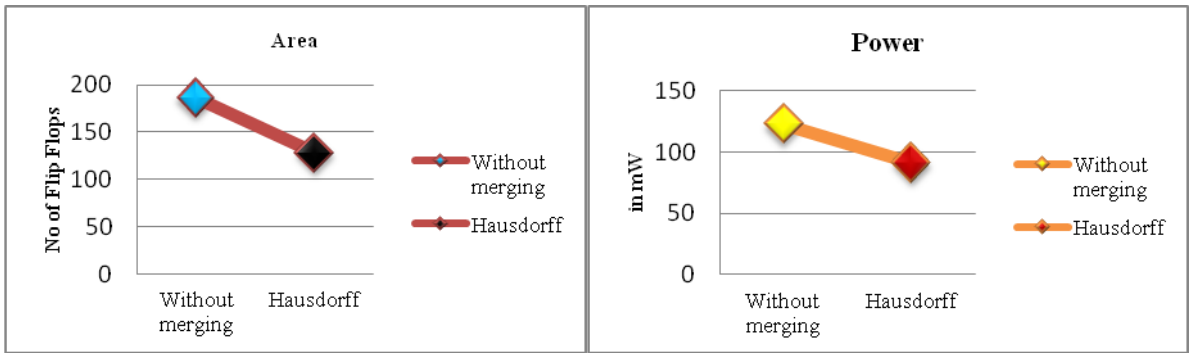
Figure 11. Peak memory usage before and after using algorithm

V. PERFORMANCE ANALYSIS

A. *Mean – Squared Error(MSE)*

This section demonstrates the performance analysis for various parameters during the implementation. Figure 12(a) shows that number of flip flop is being reduced. Likewise power is optimized in Figure 12(b).

(a) (b)



The delay is reduced which is graphically represented in Figure12(c). Peak memory usage has been reduced which is described in Figure12(d).

(c) (d)

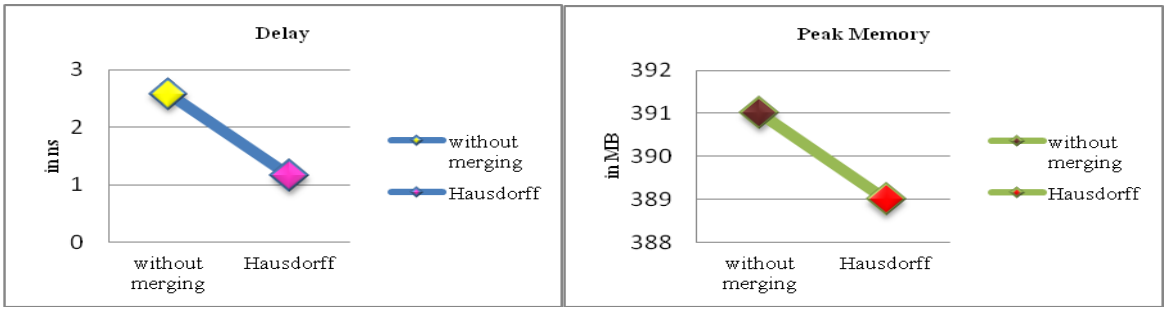


Figure 12. (a),(b),(c) and (d) Graphical representation of performance analysis

TABLE I. SYNTHESIS ANALYSIS

FIR Circuit	Area	Power	Delay	Peak memory
Before Merging	186 FF	123 mW	2.59	391 MB
After Merging	128 FF	91 mW	1.12	389 MB

VI. CONCLUSION

In this paper we proposed an algorithm for clustering of flip flops to minimize wirelength and power reduction by merging of flip flops. The procedure includes distance calculation, which calculates distance with manhattan distance function. The concept of clustering of flip flops is done to curtail wirelength and hence combination table is built. The simulation results shows that our algorithm can reduce the memory usage and the total power is reduced upto 25.8%.

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